

IN THE CLAIMS:

1. (currently amended) In a communications system, a modified gain method for non-causal channel equalization using feed-forward and feedback compensation, the method comprising:

receiving a first bit ~~(present)~~ input;

comparing a second bit ~~(past)~~ value, received prior to the first bit input, to a third bit ~~(future)~~ value received subsequent to the first bit input;

in response to the comparisons, modifying the amplitude of the first bit input; and,

determining the value of the first bit input.

2. (currently amended) The method of claim 1 further comprising:

establishing a comparator threshold $V_{opt}[D]$ to distinguish “1” bit values from “0” bit values; and,

wherein determining the value of the first bit input includes comparing the amplitude modified first bit input to the V_{opt} threshold.

3. (original) The method of claim 2 wherein modifying the amplitude of the first bit input in response to the comparisons includes modifying the amplitude to compensate for the effect of the second and third bit values being equal.

4. (currently amended) The method of claim ~~[[3]]~~ 2 wherein comparing a second bit value to a third bit value includes only one of the second and third bit values being a “1” value; and,

wherein modifying the amplitude of the first bit input includes supplying a unity amplitude modifier in response to only one of the second and third bit values being a “1” value.

5. (currently amended) The method of claim [[4]] 2 wherein comparing a second bit value to a third bit value includes both the second and third bit values being a “1” value; and,

wherein modifying the amplitude of the first bit input includes supplying a low amplitude modifier in response to both the second and third bit values being a “1” value.

6. (currently amended) The method of claim [[5]] 2 wherein comparing a second bit value to a third bit value includes both the second and third bit values being a “0” value; and,

wherein modifying the amplitude of the first bit input includes supplying a high amplitude modifier in response to both the second and third bit values being a [[“1”]] “0” value.

7. (currently amended) The method of claim [[6]] 2 further comprising:

receiving a serial data stream;

comparing the serial data stream to the Vopt threshold to generate the third bit value;

delaying the serial data stream period to generate the first bit input; and,

delaying a previously generated first bit value to generate the second bit value.

8. (original) The method of claim 7 wherein receiving a serial data stream includes receiving a serial data stream encoded with forward error correction (FEC);

the method further comprising:

following the determination of the first bit values, FEC decoding the first bit values; and,

using the FEC corrections of the first bit values to adjust the amplitude modifier gains.

9. (currently amended) The method of claim 7 further comprising:

establishing a D1 comparator threshold to distinguish high probability "1" first bit values;

establishing a D0 comparator threshold to distinguish high probability "0" first bit values;

wherein modifying the amplitude of the first bit input includes a modification selected from a group consisting of:

supplying a unity amplitude modifier in response to only one of the second and third bit values being a "1" value;

supplying a low amplitude modifier ~~includes supplying a low amplitude modifier~~ in response to both the second and third bit values being a "1" value, where $[[Q]]z = V_{opt}/D1[D]$; and,

~~wherein supplying a high amplitude modifier includes supplying a high amplitude modifier~~ in response to both the second and third bit values being a "0" value, where $[[Q]]z = V_{opt}/D0[D]$.

10. (currently amended) The method of claim [[7]] 1 wherein receiving a serial data stream includes receiving a serial data stream selected from the group including non-return to zero (NRZ), return to zero (RZ), binary symmetric, binary asymmetric, binary communication protocols where the clock is recovered from the data stream, and binary communication protocols where the clock is supplied as an independent signal.

11. (currently amended) A modified gain non-causal channel equalization communication system using feed-forward and feedback compensation, the system comprising:

a modified gain decision circuit having an input to accept a serial data stream, an input to accept a second bit ~~(past)~~ value received prior to a first bit ~~(present)~~ input, an input to accept a third bit ~~(future)~~ value received subsequent to the first bit input, and an output to supply a first bit value responsive to the second and third bit values;

a feed-forward equalizer having an input to accept the serial data stream and an output to supply third bit values; and,

a feedback equalizer having an input to accept first bit values and an output to supply second bit values.

12. (original) The system of claim 11 wherein the modified gain decision circuit includes:

a multiplier having an input to accept first bit inputs and an output to supply amplitude modified first bit inputs; and,

a first comparator having an input to accept the amplitude modified first bit inputs, an input to accept a V_{opt} comparator threshold, and an output to supply the first bit values.

13. (original) The system of claim 12 wherein the multiplier further includes an input to accept an amplitude modifier signals;

wherein the modified gain decision circuit further includes a calculator circuit having inputs to accept the second and third bit values and an output to supply amplitude modifier signals responsive to a comparison of the second and third bit values.

14. (original) The system of claim 13 wherein the calculator circuit supplies amplitude modifier signals that compensate for the effect of the second and third bit values being equal.

15. (currently amended) The system of claim ~~[[14]]~~ 13 wherein the calculator circuit supplies a unity amplitude modifier signal in response to the only one of the second and third bit values being a “1” value.

16. (currently amended) The system of claim ~~[[15]]~~ 13 wherein the calculator circuit supplies a low amplitude modifier signal in response to both the second and third bit values being a “1” value.

17. (currently amended) The system of claim ~~[[16]]~~ 13 wherein the calculator circuit supplies a high amplitude modifier signal in response to both the second and third bit values being a “0” value.

18. (original) The system of claim 13 wherein the modified gain decision circuit receives a serial data stream encoded with forward error correction (FEC);

the system further comprising:

an FEC circuit having an input to accept first bit values and an output to supply FEC corrected first bit values;

a statistics circuit having an input to accept first bit values and FEC corrected first bit values and an output to supply corrections in response to comparing the first bit values to the FEC corrected first bit values; and,

wherein the calculator circuit supplies amplitude modified signals responsive to the corrections.

19. (original) The system of claim 13 wherein the modified gain decision circuit further includes a delay having an input to accept the serial data stream and an output to supply the first bit input delayed with respect to the serial data stream.

20. (original) The system of claim 19 wherein the feed-forward equalizer includes a second comparator having an input to accept the serial data stream, an input to accept the V_{opt} threshold, and an output to supply third bit values.

21. (original) The system of claim 20 wherein the feedback equalizer includes a latch having an input connected to the first comparator output, and an output to supply the second bit values.

22. (currently amended) The system of claim ~~[[17]]~~ 13 wherein the calculator circuit has a input to accept a D1 comparator threshold to distinguish high probability “1” first bit values, and an input to accept a D0 comparator threshold to distinguish high probability “0” first bit values; and,

wherein the calculator circuit supplies an amplitude modifier signal selected from a group consisting of a unity amplitude modifier in response to the only one of the second and third bit values being a “1” value, a low gain amplitude modifier in response to both the second and third bit values being a “1” value, where $[[Q]]z = V_{opt}/D1[D]$, and a high gain amplitude modifier, in response to both the second and third bit values being a “0” value, where $[[Q]]z = V_{opt}/D0[D]$.

23. (original) The system of claim 22 wherein the calculator circuit is a look up table (LUT) including a plurality of stored amplitude modified signals for a plurality of V_{opt} , D1, and D0 threshold values.

24. (original) The system of claim 11 wherein the modified gain circuit receives a serial data stream input selected from the group including non-return to zero (NRZ), return to zero (RZ), binary symmetric, binary asymmetric, binary communication protocols where the

clock is recovered from the data stream, and binary communication protocols where the clock is supplied as an independent signal.